TS512MLH64V1H
TS1GLH64V1H

288Pin DDR4 2133 UDIMM
4GB ~ 8GB Based on 512Mx8

Description

DDR4 Unbuffered DIMM is high-speed, low power memory module that use 512Mx8bits DDR4 SDRAM in FBGA package and a 4Kbits serial EEPROM on a 288-pin printed circuit board. DDR4 Unbuffered DIMM is a Dual In-Line Memory Module and is intended for mounting into 288-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

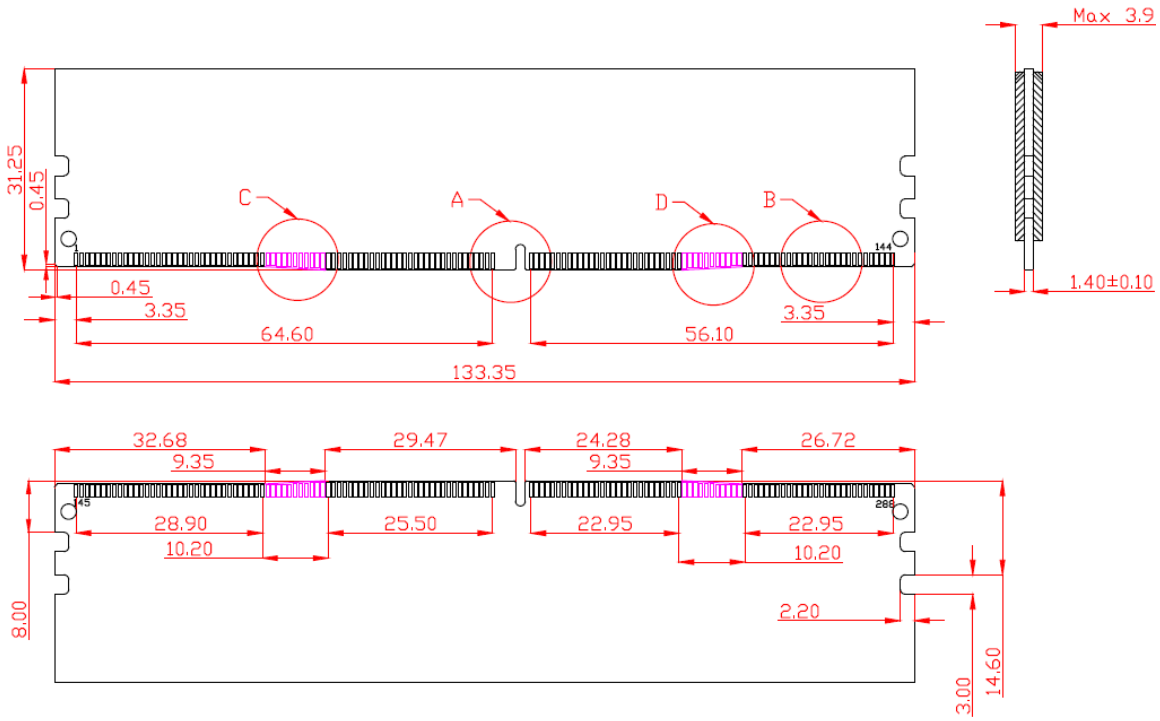
Features

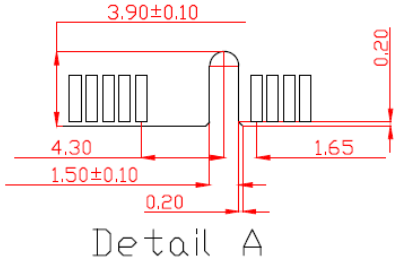
- RoHS compliant products.
- JEDEC standard 1.2V ± 0.06V power supply
- VDDQ=1.2V ± 0.06V
- Clock Freq: 1067MHZ for 2133Mb/s/Pin.
- Programmable CAS Latency: 10,11,12,13,14,15,16
- Programmable Additive Latency (Posted /CAS): 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 11, 14(DDR4-2133)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- On DIMM Thermal Sensor
- Asynchronous reset

Pin Identification

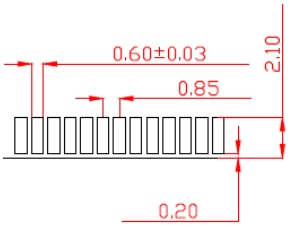
Symbol	Function
A0~A17	SDRAM address bus
BA0, BA1	SDRAM bank select
BG0, BG1	SDRAM bank group select
RAS_n	SDRAM row address strobe
CAS_n	SDRAM column address strobe
WE_n	SDRAM write enable
CS0_n, CS1_n	DIMM Rank Select Lines
CKE0, CKE1	SDRAM clock enable lines
ODT0, ODT1	SDRAM on-die termination control lines
ACT_n	SDRAM activate
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)
PARITY	SDRAM parity input
VDD	SDRAM I/O and core power supply
12 V	Optional power Supply on socket but not used on UDIMM
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD EEPROM positive power supply
SCL	I^2C serial bus clock for EEPROM
SDA	I^2C serial bus data line for EEPROM
SA0–SA2	I^2C slave address select for EEPROM
ALERT_n	SDRAM ALERT_n
VPP	SDRAM Supply
RESET_n	Set DRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use
NC	No Connection

Dimensions (Unit: millimeter)





Detail A



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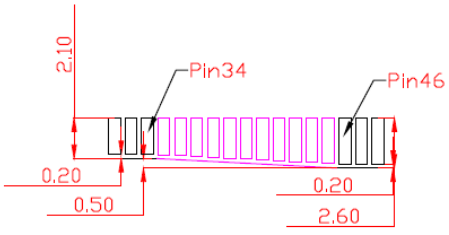

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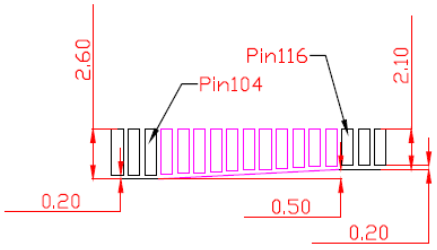


Detail D

Note:
1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

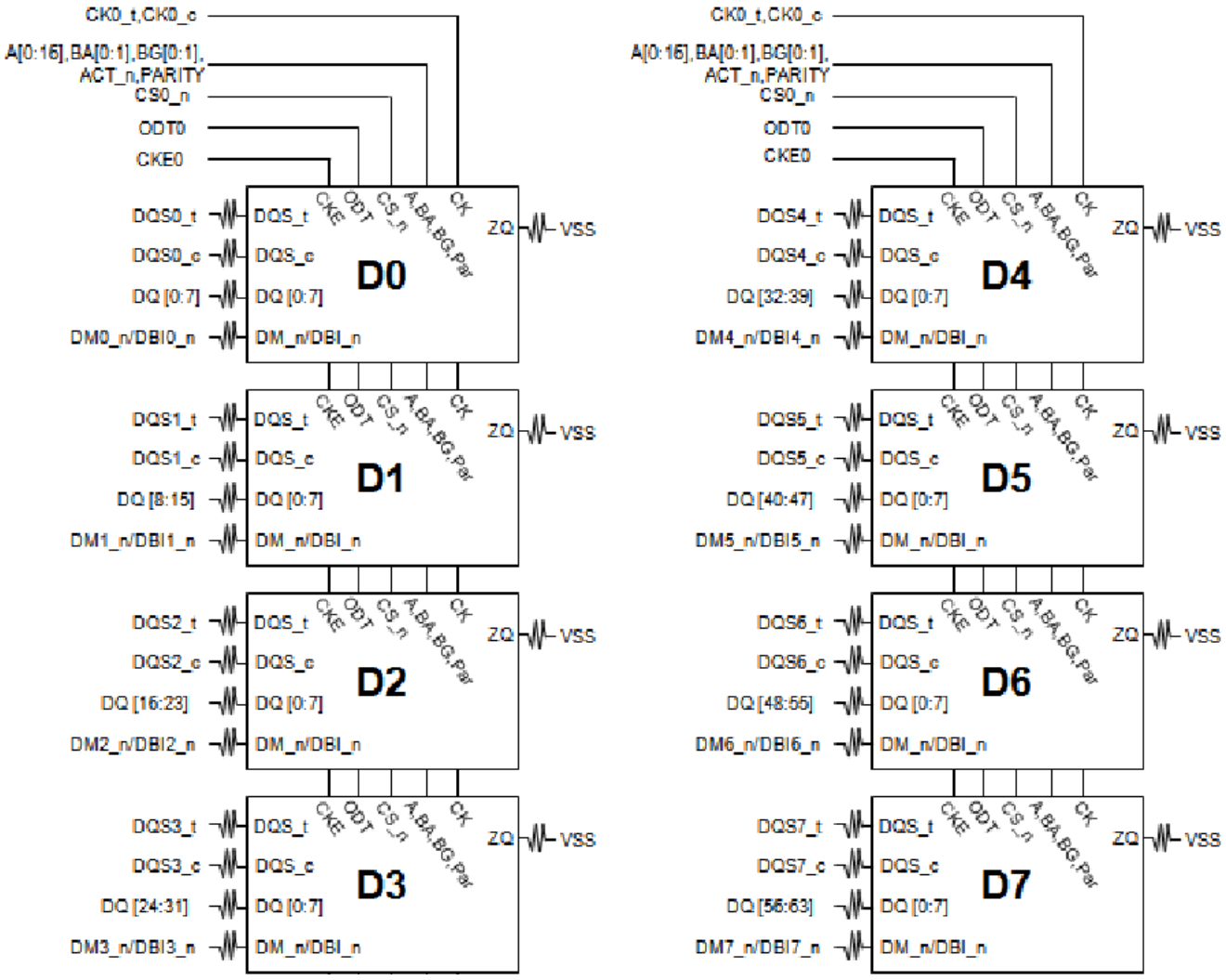
Pin Assignments

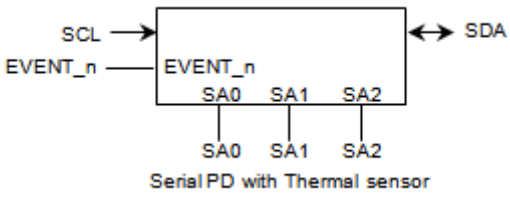
Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	NC	49	NC	97	DQ32	145	NC	193	VSS	241	VSS
02	VSS	50	VSS	98	VSS	146	VREFCA	194	NC	242	DQ33
03	DQ4	51	NC	99	NC	147	VSS	195	VSS	243	VSS
04	VSS	52	NC	100	NC	148	DQ5	196	DQS8_c	244	DQS4_c
05	DQ0	53	VSS	101	VSS	149	VSS	197	DQS8_t	245	DQS4_t
06	VSS	54	NC	102	DQ38	150	DQ1	198	VSS	246	VSS
07	NC	55	VSS	103	VSS	151	VSS	199	NC	247	DQ39
08	NC	56	NC	104	DQ34	152	DQS0_c	200	VSS	248	VSS
09	VSS	57	VSS	105	VSS	153	DQS0_t	201	NC	249	DQ35
10	DQ6	58	RESET_n	106	DQ44	154	VSS	202	VSS	250	VSS
11	VSS	59	VDD	107	VSS	155	DQ7	203	CKE1	251	DQ45
12	DQ2	60	CKE0	108	DQ40	156	VSS	204	VDD	252	VSS
13	VSS	61	VDD	109	VSS	157	DQ3	205	RFU	253	DQ41
14	DQ12	62	ACT_n	110	NC	158	VSS	206	VDD	254	VSS
15	VSS	63	BG0	111	NC	159	DQ13	207	BG1	255	DQS5_c
16	DQ8	64	VDD	112	VSS	160	VSS	208	ALERT_n	256	DQS5_t
17	VSS	65	A12/BC_n	113	DQ46	161	DQ9	209	VDD	257	VSS
18	NC	66	A9	114	VSS	162	VSS	210	A11	258	DQ47
19	NC	67	VDD	115	DQ42	163	DQS1_c	211	A7	259	VSS
20	VSS	68	A8	116	VSS	164	DQS1_t	212	VDD	260	DQ43
21	DQ14	69	A6	117	DQ52	165	VSS	213	A5	261	VSS
22	VSS	70	VDD	118	VSS	166	DQ15	214	A4	262	DQ53
23	DQ10	71	A3	119	DQ48	167	VSS	215	VDD	263	VSS
24	VSS	72	A1	120	VSS	168	DQ11	216	A2	264	DQ49
25	DQ20	73	VDD	121	NC	169	VSS	217	VDD	265	VSS
26	VSS	74	CK0_t	122	NC	170	DQ21	218	CK1_t	266	DQS6_c
27	DQ16	75	CK0_c	123	VSS	171	VSS	219	CK1_c	267	DQS6_t
28	VSS	76	VDD	124	DQ54	172	DQ17	220	VDD	268	VSS
29	NC	77	VTT	125	VSS	173	VSS	221	VTT	269	DQS5
30	NC	78	EVENT_n	126	DQ50	174	DQS2_c	222	PARITY	270	VSS
31	VSS	79	A0	127	VSS	175	DQS2_t	223	VDD	271	DQ51
32	DQ22	80	VDD	128	DQ60	176	VSS	224	BA1	272	VSS
33	VSS	81	BA0	129	VSS	177	DQ23	225	A10/AP	273	DQ61
34	DQ18	82	RAS_n/A16	130	DQ56	178	VSS	226	VDD	274	VSS
35	VSS	83	VDD	131	VSS	179	DQ19	227	RFU	275	DQ57
36	DQ28	84	CS0_n	132	NC	180	VSS	228	WE_n/A14	276	VSS
37	VSS	85	VDD	133	NC	181	DQ29	229	VDD	277	DQS7_c
38	DQ24	86	CAS_n/A15	134	VSS	182	VSS	230	NC	278	DQS7_t
39	VSS	87	ODT0	135	DQ62	183	DQ25	231	VDD	279	VSS
40	NC	88	VDD	136	VSS	184	VSS	232	A13	280	DQ63
41	NC	89	CS1_n	137	DQ58	185	DQS3_c	233	VDD	281	VSS
42	VSS	90	VDD	138	VSS	186	DQS3_t	234	NC	282	DQ59
43	DQ30	91	ODT1	139	SA0	187	VSS	235	NC	283	VSS
44	VSS	92	VDD	140	SA1	188	DQ31	236	VDD	284	VDDSPD
45	DQ26	93	NC	141	SCL	189	VSS	237	NC	285	SDA
46	VSS	94	VSS	142	VPP	190	DQ27	238	SA2	286	VPP
47	NC	95	DQ36	143	VPP	191	VSS	239	VSS	287	VPP
48	VSS	96	VSS	144	RFU	192	NC	240	DQ37	288	VPP

Note:

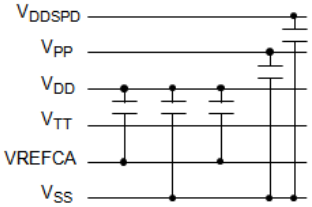
1. VPP is 2.5V DC.
2. Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs.
3. Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
4. The 5th VPP is required on all modules, DIMMs.

Block Diagram
4GB, 512Mx64 Module(1 Rank x8)

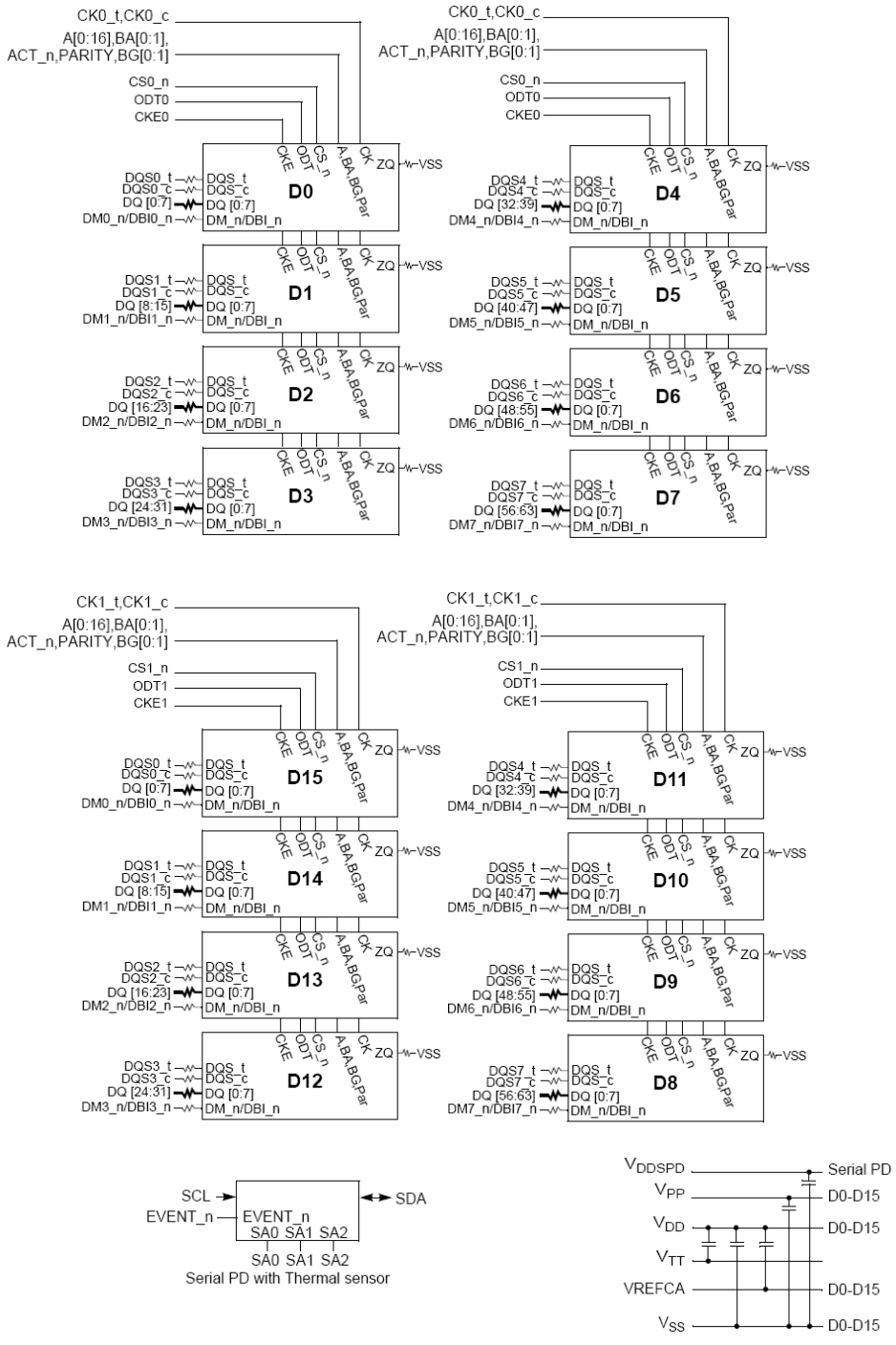




Serial PD with Thermal sensor



Block Diagram
8GB, 1Gx64 Module(2 Rank x8)



Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note:
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. At 0 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.3 ~ 1.5	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.3 ~ 1.5	V	1
Voltage on VPP pin relative to Vss	VPP	-0.3 ~ 3.0	V	3
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.5	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VPP must be equal or greater than VDD/VDDQ at all times.

AC & DC Operating Conditions

Recommended DC operating conditions (SSTL –1.5)

Parameter	Symbol	Rating			Unit	Notes
		Min	Typ.	Max		
Supply voltage	VDD	1.14	1.2	1.26	V	1, 2
Supply voltage for Output	VDDQ	1.14	1.2	1.26	V	1, 2
Wordline supply voltage	VPP	2.375	2.5	2.75	V	3

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz

Single-ended AC & DC input levels for Command and Address

Parameter	Symbol	DDR4-1600/1866/2133		Unit	Note
		Min	Max		
I/O Reference Voltage (CMD/ADD)	VREFCA(DC)	0.49*VDDQ	0.51*VDDQ	V	1,2
DC Input Logic High	VIH(DC)	VREF+0.075	VDD	V	
DC Input Logic Low	VIL(DC)	VSS	VREF-0.075	V	
AC Input Logic High	VIH(AC)	VREF+0.1	Note 1	V	
AC Input Logic Low	VIL(AC)	Note 1	VREF-0.1	V	

Note:
1. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV)
2. For reference : approx. VDD/2 ± 12mV

Differential AC and DC Input Levels

Parameter	Symbol	DDR4-1600/1866/2133		Unit	Note
		Min	Max		
differential input high DC	VIHdiff(DC)	+0.150	NOTE 3	V	1
differential input low DC	VILdiff(DC)	NOTE 3	-0.150	V	1
differential input high AC	VIHdiff(AC)	2 x (VIH(AC) - VREF)	NOTE 3	V	2
differential input low AC	VILdiff(AC)	NOTE 3	2 x (VIL(AC) -VREF)	V	2

Note:
1. Used to define a differential signal slew-rate.
2. for CK_t - CK_c use VIH.CA/VIL.CA(AC) of ADD/CMD and VREFCA;
3. These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits (VIH.CA(DC) max, VIL.CA(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Single-ended AC & DC output levels

Parameter	Symbol	DDR4-1600/1866/2133	Unit	Note
DC output high measurement level	VOH(DC)	1.1 x VDDQ	V	
DC output mid measurement level	VOM(DC)	0.8 x VDDQ	V	
DC output low measurement level	VOL(DC)	0.5 x VDDQ	V	
AC output high measurement level	VOH(AC)	(0.7 + 0.15) x VDDQ	V	1
AC output low measurement level	VOL(AC)	(0.7 - 0.15) x VDDQ	V	1

Note:
1. The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.

Differential AC & DC output levels

Parameter	Symbol	DDR4-1600/1866/2133	Unit	Note
AC differential output high measurement level	VOHdiff(AC)	+0.3 x VDDQ	V	1
AC differential output low measurement level	VOLdiff(AC)	-0.3 x VDDQ	V	1

Note:
1. The swing of ± 0.3 × VDDQ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ at each of the differential outputs.

IDD Specification parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

4GB, 512Mx64 Module(1 Rank x8)

Parameter	Symbol	DDR4 2133 CL15	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	TBD	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	TBD	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	TBD	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	TBD	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	TBD	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	TBD	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	TBD	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	TBD	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	TBD	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	TBD	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	TBD	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	TBD	mA

Note: 1.Module IDD was calculated on the specific brand DRAM(2Xnm) component IDD and can be differently measured according to DQ loading capacitor.

8GB, 1Gx64 Module(2 Rank x8)

Parameter	Symbol	DDR4 2133 CL15	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	TBD	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	TBD	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	TBD	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	TBD	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	TBD	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	TBD	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	TBD	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	TBD	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	TBD	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	TBD	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	TBD	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	TBD	mA

Note: 1.Module IDD was calculated on the specific brand DRAM(2Xnm) component IDD and can be differently measured according to DQ loading capacitor.

Timing Parameters & Specifications

Speed		DDR4 2133		Unit
Parameter	Symbol	Min	Max	
Average Clock Period	tCK	0.938	<1.071	ns
CK high-level width	tCH	0.48	0.52	tCK
CK low-level width	tCL	0.48	0.52	tCK
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	TBD	tCK/2
DQS_t,DQS_c to DQ Skew determin-istic, per group, per access	tDQSQ	-	TBD	tCK/2
DQ output hold time from DQS_t,DQS_c	tQH	TBD	-	tCK/2
DQ output hold time deterministic from DQS_t, DQS_c	tQH	TBD	-	UI
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	TBD	UI
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH	TBD	-	UI
DQ to DQ offset , per group, per ac-cess referenced to DQS_t, DQS_c	tDQSQ	TBD	TBD	UI
DQS_t, DQS_c differential READ Pre-amble (2 clock preamble)	tRPRE	0.9	TBD	tCK
DQS_t, DQS_c differential READ Postamble	tRPST	TBD	TBD	tCK
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	TBD	TBD	tCK
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-360	180	ps
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	180	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK
Delay from start of internal write trans-action to internal read command for different bank group	tWTR_S	Max(2nCK, 2.5ns)	-	
Delay from start of internal write trans-action to internal read command for same bank group	tWTR_L	Max(4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	8	-	nCK
CAS_n to CAS_n command delay for same bank group	tCCD_L	6	-	nCK

Speed		DDR4 2133		Unit
Parameter	**Symbol**	**Min**	**Max**	
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK
Auto precharge write recovery + precharge time	tDAL	tWR+tRP/tCK		nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK,3.7ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S (1/ 2K)	Max(4nCK,3.7ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L (1/ 2K)	Max(4nCK,5.3ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 15ns)	-	ns
Power-up and RESET calibration time	tZQinit	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	nCK
Normal operation short calibration time	tZQCS	128	-	nCK
Exit Self Refresh to commands not re-quiring a locked DLL	tXS	tRFC(min)+ 10ns	-	
Exit Self Refresh to commands requir-ing a locked DLL	tXSDLL	tDLLK(min)	-	
Internal READ Command to PRE-CHARGE Command delay	tRTP	Max(4nCK,7.5ns)	-	
Minimum CKE low width for Self re-fresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	Max (4nCK,6ns)	-	
CKE minimum pulse width	tCKE	Max (3nCK,5ns)	-	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	tCK

SERIAL PRESENCE DETECT SPECIFICATION

TS512MLH64V1H Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage	CRC:0-255Byte SPD Byte use: 512Byte SPD Byte total: 512Byte	24
1	SPD Revision	-	-
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0C
3	Key Byte / Module Type	UDIMM	02
4	SDRAM Density and Banks	4Gb, 16banks	84
5	SDRAM Addressing	ROW:15, Column:10	19
6	SDRAM Package Type	-	-
7	SDRAM Optional Features	-	-
8	SDRAM Thermal and Refresh Options	-	-
9	Other SDRAM Optional Features	-	-
10	Reserved	-	00
11	Module Nominal Voltage, VDD	1.2V	03
12	Module Organization	1Rank, 8bits	01
13	Module Memory Bus Width	Non ECC, 64bits	03
14	Module Thermal Sensor	Support	80
15-16	Reserved	-	00
17	Timebases	-	00
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0.938ns	08
19	SDRAM Maximum Cycle Time (tCKAVGmax)	1.5ns	0C
20-23	CAS Latencies Supported	10, 11, 12, 13, 14, 15, 16	-
24	Minimum CAS Latency Time (tAAmin)	13.5ns	6C
25	Minimum RAS to CAS Delay Time (tRCDmin)	13.5ns	6C
26	Minimum Row Precharge Delay Time (tRPmin)	13.5ns	6C
27	Upper Nibbles for tRASmin and tRCmin	-	11
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	33ns	08
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	46.5ns	74
30-31	Minimum Refresh Recovery Delay Time (tRFC1min)	260ns	20,08
32-33	Minimum Refresh Recovery Delay Time (tRFC2min)	160ns	00,05
34-35	Minimum Refresh Recovery Delay Time (tRFC4min)	110ns	70,03
36-37	Minimum Four Activate Window Delay Time (tFAWmin)	21ns	00,A8
38	Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	3.7ns	1E
39	Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	5.3ns	2B
40	Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	5.355ns	2B
41-59	Reserved	-	00
60-77	Connector to SDRAM Bit Mapping	-	-

78-116	Reserved	-	00					
117	Fine Offset for Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	-	ED					
118	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	-	B5					
119	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	-	CE					
120	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	-	00					
121	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	-	00					
122	Fine Offset for Minimum RAS to CAS Delay Time (tRCDmin)	-	00					
123	Fine Offset for Minimum CAS Latency Time (tAAmin)	-	00					
124	Fine Offset for SDRAM Maximum Cycle Time (tCKAVGmax)	-	00					
125	Fine Offset for SDRAM Minimum Cycle Time (tCKAVGmin)	-	C2					
126-127	Cyclical Redundancy Code	-	-					
128	Raw Card Extension, Module Nominal Height	32mm	11					
129	Module Maximum Thickness	Planar Single Sides	01					
130	Reference Raw Card Used	Revision 0, Raw card A	00					
131	Address Mapping from Edge Connector to DRAM	Standard	00					
132-253	Reserved	-	00					
254-255	Cyclical Redundancy Code (CRC)	-	-					
256-319	Reserved	-	00					
320-321	Module Manufacturer ID Code	Transcend	01,4F					
322	Module Manufacturing Location	Taipei	54					
323-324	Module Manufacturing Date	-	00					
325-328	Module Serial Number	-	00					
329-348	Module Part Number	TS512MLH64V1H	54	53	35	31	32	
			4D	4C	48	36	34	
			56	31	48	20	20	
			20	20	20	20	20	
349	Module Revision Code	-	00					
350-351	DRAM Manufacturer ID Code	By Manufacturer	Variable					
352	DRAM Stepping	-	00					
353-381	Manufacturer Specific Data	By Manufacturer	Variable					
382-383	Reserved	-	00					
384-551	End User Programmable	-	-					

TS1GLH64V1H Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage	CRC:0-255Byte SPD Byte use: 512Byte SPD Byte total: 512Byte	24
1	SPD Revision	-	-
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0C
3	Key Byte / Module Type	UDIMM	02
4	SDRAM Density and Banks	4Gb, 16banks	84
5	SDRAM Addressing	ROW:15, Column:10	19
6	SDRAM Package Type	-	-
7	SDRAM Optional Features	-	-
8	SDRAM Thermal and Refresh Options	-	-
9	Other SDRAM Optional Features	-	-
10	Reserved	-	00
11	Module Nominal Voltage, VDD	1.2V	03
12	Module Organization	1Rank, 8bits	09
13	Module Memory Bus Width	Non ECC, 64bits	03
14	Module Thermal Sensor	Support	80
15-16	Reserved	-	00
17	Timebases	-	00
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0.938ns	08
19	SDRAM Maximum Cycle Time (tCKAVGmax)	1.5ns	0C
20-23	CAS Latencies Supported	10, 11, 12, 13, 14, 15, 16	-
24	Minimum CAS Latency Time (tAAmin)	13.5ns	6C
25	Minimum RAS to CAS Delay Time (tRCDmin)	13.5ns	6C
26	Minimum Row Precharge Delay Time (tRPmin)	13.5ns	6C
27	Upper Nibbles for tRASmin and tRCmin	-	11
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	33ns	08
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	46.5ns	74
30-31	Minimum Refresh Recovery Delay Time (tRFC1min)	260ns	20,08
32-33	Minimum Refresh Recovery Delay Time (tRFC2min)	160ns	00,05
34-35	Minimum Refresh Recovery Delay Time (tRFC4min)	110ns	70,03
36-37	Minimum Four Activate Window Delay Time (tFAWmin)	21ns	00,A8
38	Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	3.7ns	1E
39	Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	5.3ns	2B
40	Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	5.355ns	2B
41-59	Reserved	-	00
60-77	Connector to SDRAM Bit Mapping	-	-
78-116	Reserved	-	00

117	Fine Offset for Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	-	ED					
118	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	-	B5					
119	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	-	CE					
120	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	-	00					
121	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	-	00					
122	Fine Offset for Minimum RAS to CAS Delay Time (tRCDmin)	-	00					
123	Fine Offset for Minimum CAS Latency Time (tAAmin)	-	00					
124	Fine Offset for SDRAM Maximum Cycle Time (tCKAVGmax)	-	00					
125	Fine Offset for SDRAM Minimum Cycle Time (tCKAVGmin)	-	C2					
126-127	Cyclical Redundancy Code	-	-					
128	Raw Card Extension, Module Nominal Height	32mm	11					
129	Module Maximum Thickness	Planar Double Sides	11					
130	Reference Raw Card Used	Revision 0, Raw card B	01					
131	Address Mapping from Edge Connector to DRAM	Mirrored	01					
132-253	Reserved	-	00					
254-255	Cyclical Redundancy Code (CRC)	-	-					
256-319	Reserved	-	00					
320-321	Module Manufacturer ID Code	Transcend	01,4F					
322	Module Manufacturing Location	Taipei	54					
323-324	Module Manufacturing Date	-	00					
325-328	Module Serial Number	-	00					
329-348	Module Part Number	TS1GLH64V1H	54	53	31	47	4C	
			48	36	34	56	31	
			48	20	20	20	20	
			20	20	20	20	20	
349	Module Revision Code	-	00					
350-351	DRAM Manufacturer ID Code	By Manufacturer	Variable					
352	DRAM Stepping	-	00					
353-381	Manufacturer Specific Data	By Manufacturer	Variable					
382-383	Reserved	-	00					
384-551	End User Programmable	-	-					